Quality fanless computers

Fitlet GPIO Connector

User guide

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CompuLab Ltd.
17 HaYetsira St., Yokneam Elite 20692,
P.O.B 687
ISRAEL
Tel: +972-4-8290100
http://www.compulab.co.il
http://fit-pc.com/web/
Fax: +972-4-8325251

Revision History

Revision	Author/Engineer	Revision Changes
0.99	Maxim Birger	Preliminary release
1.0	Maxim Birger	Initial public release

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1 Introduction

1.1 About This Document

This document is part of a set of reference documentation necessary to operate fitlet optional periphery, as GPIOs and interfaces available.

1.2 Related Documents

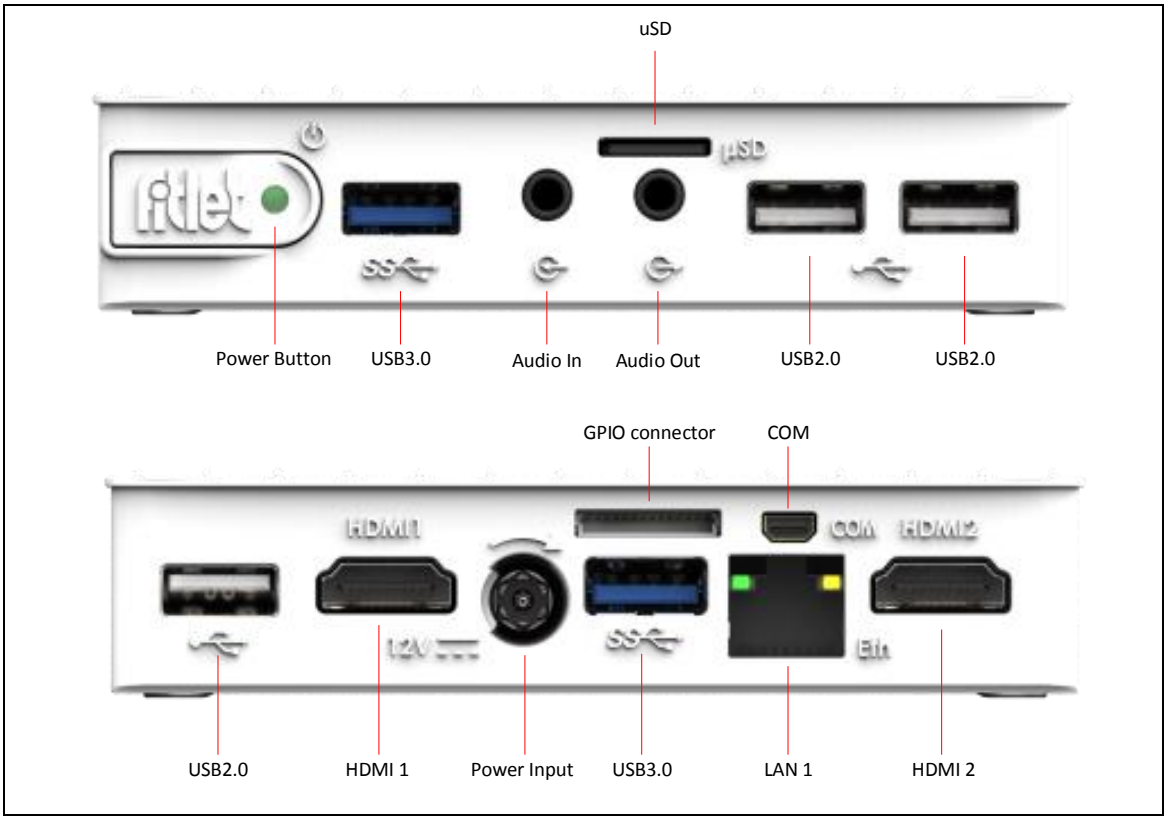
Document	Link

2 Fitlet GPIO Connector

2.1 Fitlet Port View

Fitlet front and back panel ports shown in the figure below.

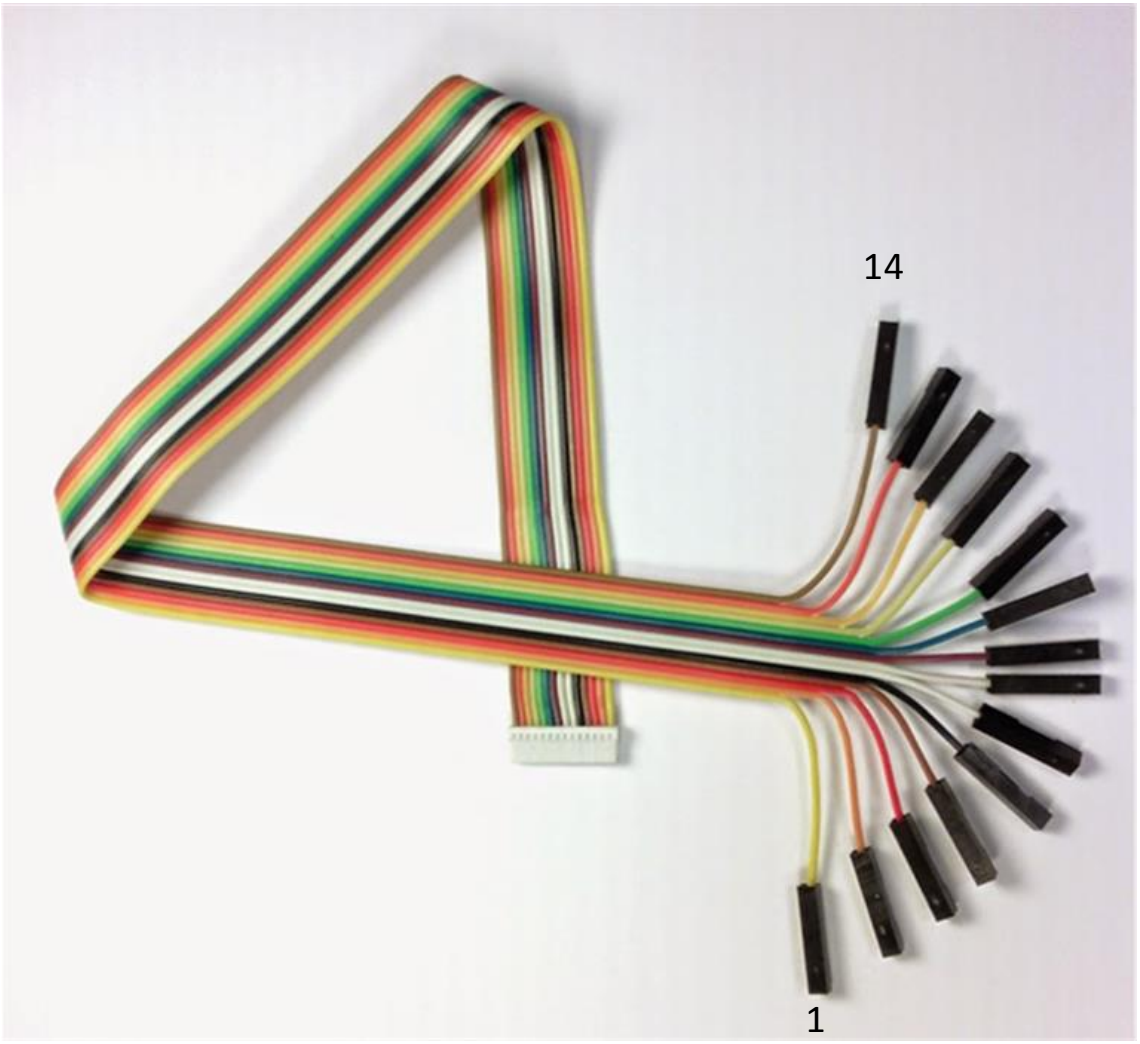
Figure 1 – fitlet front/back panel ports



2.2 Ribbon Cable

The ribbon cable provides easy GPIO connection and signals spreading. On one end it connects to GPIO connector and on the other spreads each signal to its own 1x1 header.

Figure 2 – fitlet GPIO ribbon cable



3 GPIO Configuration

3.1 GPIO Connector Pinout and Color Map

Fitlet GPIO connector (P49) pinout, as well as signal drivers/receivers with the default and configured function provided below.

Table 1 – GPIO connector pinout

GPIO Connector		Source Driver/Receiver	Source Pin number	Default function (at power up)	Signal/GPIO
Pin number	Color code				
1		SoC	BA29	GPIO	GPIO32
2			AY29	CLK_REQG_L	GPIO65
3			AY28	GPIO	GPIO50
4			BA28	GPIO	GPIO51
5			AL2	AZ_SDIN3	GPIO170
6			AU25	SCLK0	SCLK0
7			AV25	SDATA0	SDATA0
8			AY26	GPIO	GPIO69
9			AK1	AZ_SDIN1	GPIO168
10			AM1	AZ_SDIN2	GPIO169
11			AV15	IR_LED_L	GPIO184
12		Super IO controller			COM2_RX
13					COM2_TX
14					GND

3.2 GPIO Configuration Table

GPIO configuration table maps the available signals voltage, functionality, direction and other characteristics in default state (power up) and BIOS configured state.

Figure 3 – fitlet GPIO configuration table

Pin Functionality	Voltage/Power domain		Functionality		GPIO Direction		Pull (PU/PD)
GPIO	**Voltage**	**Power domain**	**BIOS**	**Default**	**BIOS**	**Default**	**BIOS**
GPIO32	3.3V	S0	F2	In	In	PU	PU
GPIO65	3.3V	S0	F1	In	In	PU	PU
GPIO50	3.3V	S0	F2	In	Out High	PU	PU
GPIO51	3.3V	S0	F2	In	Out High	No Pull	PU
GPIO170	3.3V	S5	F1	In	In	PD	PD
SCLK0	3.3V		I^2C Clock				
SDATA0	3.3V		I^2C Data				
GPIO69	3.3V		F2		Out Low		PD
GPIO168	3.3V	S5	F1	In	In	PD	PD
GPIO169	3.3V	S5	F1	In	In	PD	PD
GPIO184	3.3V	S5	F1	In	In	PU	PU
COM2_RX	3.3V	3.3V	UART Rx				
COM2_TX	3.3V	3.3V	UART Tx				
GND	GND						

Note: GPIO BIOS configuration settings are subject to changes. Please refer to up to date document for the latest information.

Warning: Proper ESD protection required to eliminate damage when operating fitlet with external hardware. Proper grounding required to provide stable signaling and avoid damage.

Do NOT operate the interface unless you know what you're doing!